BINARY/DECIMAL SPECIAL DIVIDER FOR FROQUENCY SYNTHESIS

GENERAL DESCRIPTION

The integrated circuits MMC 382 and MMC 383 are designed in order to form (either of them) with the IC MMC 381 the central unit of a phase locked loop (PLL) frequency synthesis system. If necessary the system may be microprocessor controlled.
The integrated circuit MMC 382/383, together with a prescater form a fully programmable divider. For that it generates feedback signales for a 2 or 4 modulus prescaler. The integrated circuit MMC382/383 contains a phase and freqvency comparator.
In this the divided frequency is compared with the reference frequence (likely generated by MMC 381), resulting an error signal which properly processed and filtered, controls the VCO.

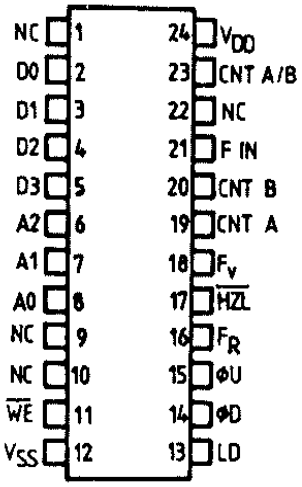
FEATURES

- Maximum input signal frequency: ≥9 MHz (V_{DD} =15 V)
- Control signals for a 2 modulus prescaler (up to 128/129) or for a 4-modules prescaler (typically 100/101/110/111), selectable by user.
- Binary (MMC 383) or decimal (382) programming of the dividing rates;
- In decimal configuration (MMC 382) the circuit can be manually programmed with 10 position multiplexed switches (BCD coded).
- It is included a phase and frequency comparator wich can be disabled by user with outputs in high Z state.
- High noise imunity
- Low supply current (<2.5 mA/V_{DD}=5 V for any dividing rates with t_{FIN}=3 MHz)
- Wide power supply voltage range: 3÷18 V

APPLICATIONS

- Telecommunication systems: radio stations, radiotelephones, radiotelegraphy, professional radioreceivers.
- Programmable dividing in control systems
- Equal frequency and different filling factors signals generation

CONNECTION DIAGRAM



PIN DESIGNATION

PIN		FUNCTION
NUMBER	NAME	
1	NC	Not connected
2, 3, 4, 5	DØ ÷ D3	Data inputs
6, 7, 8	A2, A1, AØ	Address inputs
9, 10	NC	Not connected
11	$\overline{WE}$	Write enable input
12	V_{SS}	Negative supply
13	LD	Open-drain, lock detected output
14,15	$Ø_D$, $Ø_U$	Open-drain, phase-down and phase-up indication outputs
16	F_R	Reference frequency input
17	$\overline{HZL}$	High-Z lock of $Ø_U$, $Ø_D$, LD input
18	F_V	Divided frequency output
19	CNTA	2 or 4-modulus prescaler feedback signal output
20	CNTB	4-modulus prescaler feedback signal output
21	F_{IN}	Input for the signal from the prescaler
22	NC	Not connected
23	CNT A/B	2 or 4-modules prescaler selecting signal input
24	V_{DD}	Positive supply

ABSOLUTE MAXIMUM RATINGS

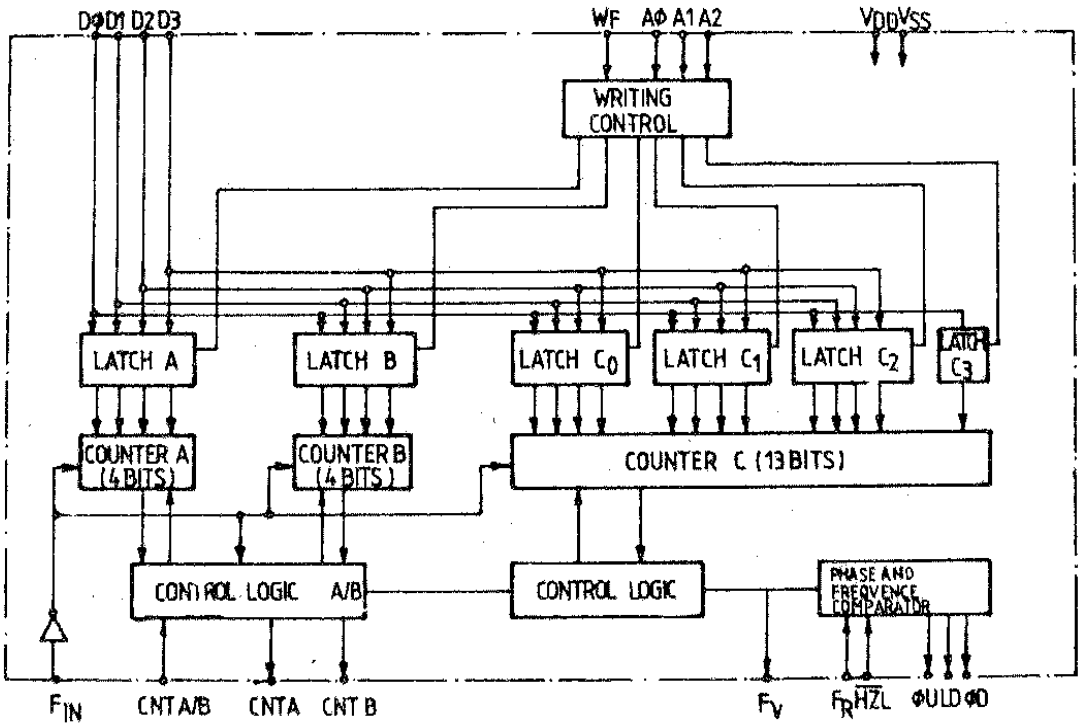
V_{DD}*	Supply voltage: G and H types	-0.5 to	20	V
	E and F types	-0.5 to	18	V
V_I	Input voltage	-0.5 to	V_{DD}+0.5	V
I_I	DC input current (any one input)		±10	mA
P_{tot}	Total power dissipation (per package)		200	mW
	Dissipation per output transistor for T_A = full package-temperature range		100	mW
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C
T_{stg}	Storage temperature	-65 to	150	°C

* All voltage values are referred to V_{SS} pin voltage

RECOMMENDED OPERATING CONDITIONS

V_{DD}*	Supply voltage: G and H types	3 to	18	V
	E and F types	3 to	15	V
V_I	Input voltage	0 to	V_{DD}	V
T_A	Operating temperature : G and H types	-55 to	125	°C
	E and F types	-40 to	85	°C

BLOCK DIAGRAM



DATA MAP

WORD	A2	A1	A0	D3	D2	D1	D0	LATCH
1.	0	0	0	A3	A2	A1	A0	A
2.	0	0	1	B3	B2	B1	B0	B
3.	0	1	0	C03	C02	C01	C00	C0
4.	0	1	1	C13	C12	C11	C10	C1
5.	1	0	0	C23	C22	C21	C20	C2
6.	1	0	1	X	X	X	C30	C3
7.	1	1	0	X	X	X	X	—
8.	1	1	1	X	X	X	X	—

X = DON'T CARE

FUNCTIONAL DESCRIPTION

The programmable dividing block of the VCO's frequency

This stage consists of two 4 bit programmable counters (A and B), a 13 bit programmable counter (C) and control logic. Each counter has a latch-typ memory for the inserted programmed numbers (see data map).

The address inputs A0—A2 select only one internal latch wich stores the dates at inputs D0—D3 during the "low" level of the write enable signal WE.

The C counter of MMC 382 is $3^1/_2$ digit decimal counter with a dividing ratio between 2 and 2001.

The C counter of MMC 383 is a 13 bit binary counter with a dividing ratio between 2 and 8193.

When CNT A/B is "low" the A and B counters operate separately with a clock signal from the F_{IN} input, generating two output signals (CNT A and CNT B) for a 4 modulus prescaler.

At the beginning of a dividing cycle the outputs CNT A and CNT B are "low" and remain in this state for a number of clock periods equal to the programmed then the outputs pass to "high" until the end of the dividing cycle of the C counter.

The F_V output is "high" excepting a single period of the signal applied to the input F_{IN} when it passes to "low" pointing out the end of a cycle of the C counter and loading of the programmed numbers of the internal memories in the A, B, C counters.

In order to have a correct dividing, the numbers programmed for each counter should satisfy the following conditions:

$$C \geq A+1 \qquad \text{and} \qquad C \geq B+1$$

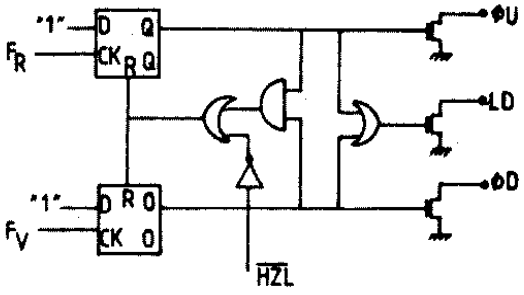
By means of a 100/101/110/111 prescaler the dividing ratio is obtained:

$$N = A + 10B + 100C$$

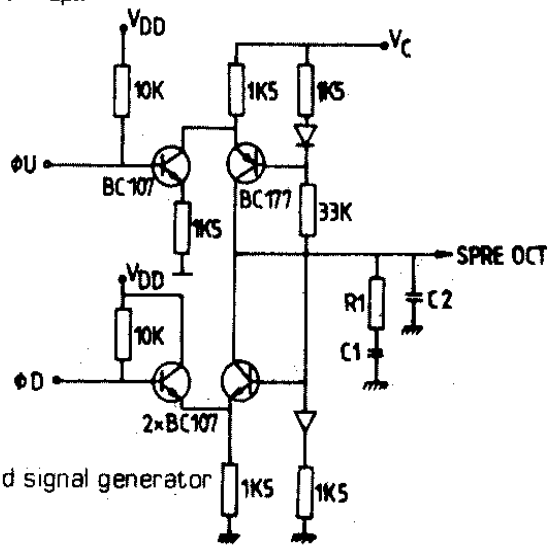
With $C \geq 10$ it is posible to obtain any dividing state in the range of:

1000÷200,199 for MMC 382
1000÷819,399 for MMC 383

When the CNT A/B input is "high" the A and B counters are together forming a 7 bit (E) programmable counter. In this case the first cell of the B counter is not used. In the E counter the most significant bit (MSB) is B_3 and the last significant bit (LSB) is A_0 (see data map).



Phase and frequency comparator



VCO command signal generator

The E counter delivers a control signal al the CNT A output for a prescaler with 2 dividing ratioes P/P+1, where $P \leq 128$.

In order to have a correct dividing the numbers programmed for each counter should satisfy the condition $C \geq E+1$.

By means of a P/P+1 prescaler it is possible to obtain a dividing ratio $N = E + C \times P$.

By means of a 128/129 prescaler and $C \geq 128$ it is possible to obtain any dividing ratio in the range of:

$2^7 = 128 \div 256,255$ for MMC 382
$2^7 = 128 \div 2^{20} + 2^8 - 1 = 1,048,831$ for MMC 383

Phase and frequency comparator

An internal output of the C counter (which externally goes to the pin F_V) and the F_R input (connected to the reference signal divider of the circuit MMC 381) are connected to a phase and frequency comparator. This generates signals at 3 open drain outputs: U, D and LD.

When the input signals are in phase the outputs ϕ_U, ϕ_D and LD are in a high-Z state, excepting very narrow pulses (<100ns) at V_{SS}.

When the input signals are not in phase, and the outputs ϕ_U, ϕ_D and LD are connected through resistances at V_{DD}, the mean voltage at the outputs ϕ_U, ϕ_D provides information about the phase and frequency error.

When $f_{FV} > f_{FR}$, the mean voltage at ϕ_U is higher than the one at ϕ_D, and viceversa. By external processing of the information it is possible to obtain a command signal for the voltage controlled oscillator (VCO); an example is shown in fig. below. As the phase and frequency error decreases in any way ($f_{FV} > f_{FR}$ or $f_{FV} < f_{FR}$) the mean voltage at the LD output increases.

A "low" signal at the HZL input inhibits the comparator, driving the outputs ϕ_U, ϕ_D and LD in high-Z state

STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER			TEST CONDITIONS				VALUES							UNIT
			V_I (V)	V_O (V)	I_O (μA)	V_{DD} (V)	T^*_{LOW}		25°C			T^*_{HIGH}		
							min.	max.	min.	typ	max.	min.	max.	
I_L	Quiescent current	G, H types	0/ 5			5		15		0.12	15		450	μA
			0/10			10		30		0.12	30		900	
			0/15			15		60		0.12	60		1800	
			0/20			20		300		0.24	300		9000	
		E, F types	0/ 5			5		50		0.12	50		450	
			0/10			10		100		0.12	100		900	
			0/15			15		200		0.12	200		1800	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5 /0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15 0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5 1.5	1	15		4			4		4	
I_{OH}	Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		3.0	6.8		-2.4		
I_{OL}	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		E, F types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	G, H types	0/18	Any input		18		±0.1		±10 [5]	±0.1		±1	μA
		E, F types	0/15			15		±0.3		±10 [5]	±0.3		±1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{LOW} = −55°C for G, H devices; −40°C for E, F devices.
* T_{HIGH} = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:
1 V min. with V_{DD} = 5 V
2 V min. with V_{DD} = 10 V
2.5 V min. with V_{DD} = 15 V

DYNAMIC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES min.	VALUES max.	UNIT
t_{PLH}, t_{PHL} Propagation delay time F_{IN} to F_V	5 10 15		300 200 120	ns
t_{PLH}, t_{PHL} Propagation delay time F_{IN} to CNTA CNTB	5 10 C_L = 15 pF 15		240 120 90	ns
t_{THL}, t_{TLH} Transition time at F_V	5 10 15		200 100 80	ns
t_{THL}, t_{TLH} Transition time at CNTA, CNTB	5 10 C_L = 15 pF 15		80 40 25	ns
f_{CL} Maximum frequency clock	5 10 15	3 6 9		MHz
t_W Minimum clock pulse width at F_{IN}	5 10 15		160 80 60	ns
t_r, t_f Rise and fall time at F_{IN}	5 10 15		15 4 1	µs
t_W Minimum pulse WE = "0" width	5 10 15		120 60 50	ns
t_{SU} Set-up time D0—D3, A0—A2 to WE	5 10 15		80 40 30	ns